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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,746	01/08/2004	Jon A. Casey	FIS920030357US1	1745

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EXAMINER	
NGUYEN, TUAN H	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 11/21/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/707,746	CASEY ET AL.
	Examiner	Art Unit
	Tuan H. Nguyen	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *19-22* is/are withdrawn from consideration.

5)☒ Claim(s) *13-18* is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/8/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group II, claims 1-18 in the reply filed on 9/15/05 is acknowledged. The traversal is on the ground(s) that "both Group I and II are one and the same, and they do not fit the criteria for restriction.". This is not found persuasive because for the reason as noted in the Restriction Requirement, the product as claimed can be made by another and materially different process such as salicide could be formed by co-sputtering metal and silicon rather than annealing to react the metal with silicon.

The requirement is still deemed proper and is therefore made FINAL.

Specification

The following title is suggested:

-- METHOD FOR INTEGRATING THERMISTOR --.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukuda et al. in view of Talwar et al..

Fukuda et al., figs. 1-6 and related text on col. 3-6 disclose the claimed method for integrating thermistor in an integrated circuit (fig. 4 and related text on col. 4) including the step of forming a thermistor 3 of silicide on an isolation region 2 as a part of the process for forming the integrated circuit (fig. 1, col. 3, lines 27-57). Fukuda et al. do not expressly disclose further steps for forming a silicide on a single crystal semiconductor.

With respect to claims 3, 4, see col. 3, lines 27-35, col. 4, lines 29-30, wherein the thermistor is of WSi and the thickness is 100 nm.

With respect to claim 6, see col. 3, lines 48-50 wherein substrate 1 is of silicon and layer 2 is of silicon dioxide.

Talwar et al., in a method for forming silicide region on an integrated circuit as shown in figs. 1A-1L and text on col. 4-9 teaches the process for forming salicide precursor layer 34 over the isolation region 20 and upper layer of single crystal semiconductor region 25 (fig. 1E, col. 6, second paragraph); reacting the salicide precursor layer 34 with the upper layer 25 to form a salicide 40 self-aligned to the upper layer 25; and removing an unreacted portion of the salicide precursor layer 34 (col. 9, second paragraph).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to have simultaneously forming salicide regions on both isolation and the single crystal semiconductor layer as suggested by Talwar et al. in Fukuda et al. process of integrating thermistor in an integrated circuit for reducing process steps, time and cost.

With respect to claims 2, 5, 7-10, both Fukuda et al. and Talwar et al. do not disclose the interlevel dielectric layer and isolation region; however, it would have been obvious to those ordinary skilled in the art to have formed isolation region by either trench isolation, field oxide or oxide layer, and used BPSG as an interlevel dielectric layer since they are well-known process and material in semiconductor processing technology for isolating the semiconductor regions or layers in an integrated circuit.

With respect to claim 12, since Talwar et al. teaches the use of silicide 42 over the isolation region 20 as a local interconnection (fig. 2), it would have been obvious to those skilled in the art at the time the invention was made to use the thermistor as a local interconnection as suggested by Talwar et al. in Fukuda et al. for simplifying the circuit, reducing the process complexity and cost.

Allowable Subject Matter

Claims 13-18 are allowed.

The following is a statement of reasons for the indication of allowable subject matter: None of the references of record teaches or suggests the claimed method for forming a thermistor including the step of etching the ILD selective to the patterned thermistor material to define openings in the ILD above the first wiring level, the thermistor material serving as a hard-mask during the etching.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Hsu, Souma, Oda, Mooney et al., and Patel et al. are cited as of interest.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuan H. Nguyen whose telephone number is 571-272-1694. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuan H. Nguyen
Primary Examiner
Art Unit 2813